IN THE CLAIMS

1. (Currently amended) A voltage boosting circuit comprising:

boosting capacitors that include a first boosting capacitor connected to a driving node and a last boosting capacitor configured to output a boosting voltage; ~~and~~

switches configured to connect the boosting capacitors in series in response to a control signal, the boosting voltage configured to vary as a voltage level at the driving node changes according to a logic state of a boosting level control signal, wherein the control signal and the boosting level control signal are able to operate independently of each other, and wherein the logic state of the boosting level control signal is configured to enter a logic high state or a logic low state in response to an external supply voltage level; and

an external supply voltage detector configured to detect the external supply voltage level and to generate the boosting level control signal.

2. (Original) The voltage boosting circuit of claim 1, configured such that when the boosting level control signal is in a first logic state, the voltage level at the driving node changes from a ground voltage level to an external supply voltage level, thus increasing the boosting voltage level.

3. (Previously presented) The voltage boosting circuit of claim 2, configured such that when the boosting level control signal is in a second logic state, the voltage level at the driving node is fixed at a ground voltage level, thus decreasing the boosting voltage level.

4. (Cancelled)

5. (Cancelled)

6. (Currently amended) A method of generating a boosting voltage in a voltage boosting circuit that includes boosting capacitors with a first boosting capacitor connected to a driving node and a last boosting capacitor that outputs the boosting voltage, and switches that connect the [[of ]]boosting capacitors in series in response to a control signal, the method comprising:

increasing the boosting voltage by changing a voltage level at the driving node from a ground voltage level to an external supply voltage level when a boosting level control signal is in a first logic state; ~~and~~

decreasing the boosting voltage by an amount approximately equal to the external supply voltage level by fixing the voltage level at the driving node to the ground voltage level when the boosting level control signal is in a second logic state, wherein the control signal and the boosting level control signal are able to operate independently of each other;

detecting the external supply voltage level and changing the boosting level control signal to the first logic state when the external supply voltage level is less than a reference voltage level; and

detecting the external supply voltage level and changing the boosting level control signal to the second logic state when the external supply voltage level is greater than the reference voltage level.

7. (Original) The method of claim 6, further comprising:

detecting the external supply voltage level and changing the boosting level control signal to the first logic state when the external supply voltage level is less than a reference voltage level; and

detecting the external supply voltage level and changing the boosting level control signal to the second logic state when the external supply voltage level is greater than the reference voltage level.

8. (New) The voltage boosting circuit of claim 1, wherein the driving node is configured to have a constant voltage during both an open and closed state of the switches.

9. (New) The voltage boosting circuit of claim 3, having N boosting capacitors, wherein N is an integer greater than 1.

10. (New) The voltage boosting circuit of claim 9, wherein the boosting level voltage is substantially equal to (N+1) multiplied by the external supply voltage level for the first logic state, and substantially equal to N multiplied by the external supply voltage level for the second logic state.

11. (New) The voltage boosting circuit of claim 1, wherein the first boosting capacitor is connected to a NOR gate.

12. (New) The voltage boosting circuit of claim 1, wherein the voltage level at the driving node is responsive to an input signal that is logically combined with the boosting level control signal.